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Solution-processable organic dielectrics for graphene electronics

Cecilia Mattevi[1,4], Florian Colléaux[2], HoKwon Kim[1], Yen-Hung Lin[2], Kyung T Park[1], Manish Chhowalla[3] and Thomas D Anthopoulos[2,4]

[1] Department of Materials, Imperial College London, London SW7 2AZ, UK
[2] Department of Physics and Centre for Plastic Electronics, Blackett Laboratory, Imperial College London, London SW7 2BW, UK
[3] Materials Science and Engineering Department, Rutgers University, Piscataway, NJ 08854, USA

E-mail: c.mattevi@ic.ac.uk and t.anthopoulos@ic.ac.uk

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Abstract
We report the fabrication, at low-temperature, of solution processed graphene transistors based on carefully engineered graphene/organic dielectric interfaces. Graphene transistors based on these interfaces show improved performance and reliability when compared with traditional SiO_2 based devices. The dielectric materials investigated include Hyflon AD (Solvay), a low-*k* fluoropolymer, and various organic self-assembled monolayer (SAM) nanodielectrics. Both types of dielectric are solution processed and yield graphene transistors with similar operating characteristics, namely high charge carrier mobility, hysteresis free operation, negligible doping effect and improved operating stability as compared to bare SiO_2 based devices. Importantly, the use of SAM nanodielectrics enables the demonstration of low operating voltage ($<|1.5|$ V), solution-processable and flexible graphene transistors with tunable doping characteristics through molecular engineering of the SAM's molecular length and terminal group. The work is a significant step towards graphene microelectronics where large-volume and low-temperature processing are required.

S Online supplementary data available from stacks.iop.org/Nano/23/344017/mmedia

(Some figures may appear in colour only in the online journal)

1. Introduction

Graphene, an atomically thin layer of sp^2 carbon atoms forming a hexagonal lattice, continues to attract significant research attention because of its unique physical properties [1, 2]. A very important characteristic of graphene, when compared to traditional inorganic semiconductors, is the absence of dangling bonds in the basal plane, which implies chemical inertness and thus the possibility to process the material from solution [3–7] at low temperatures onto the surface of virtually any substrate material [8]. The latter characteristic is very important as it enables integration of graphene with various organic materials (e.g. dielectrics, semiconductors and conductors) to produce functional optoelectronic structures. To date, graphene has been utilized successfully in numerous applications, a few of which include high charge carrier mobility transistors [9] and electrically conductive electrodes [10]. However, in order to fully explore the potential of graphene materials, the development of facile routes to high performance optoelectronics would be required.

Here, we report the development of high performance, solution processed graphene transistors utilizing unconventional organic gate dielectrics that can be processed at temperatures below 150 °C. Graphene has been processed from solution onto a novel fluoropolymer gate dielectric as well as onto various self-assembled monolayer (SAM) nanodielectrics functionalized directly onto the gate electrodes. Graphene/fluoropolymer based transistors show superior electrical properties as compared to SiO_2 based devices, while transistors based on SAM nanodielectrics are shown to

[4] Authors to whom any correspondence should be addressed.

operate at ultra-low voltages (<|1.5| V) and exhibit highly controllable doping characteristics. The improved transistor performance is attributed to the very thin nature of the highly compatible interface formed between the graphene and the organic dielectrics. The simplicity, the low-temperature processing and the scalability of this approach pave the way towards flexible graphene electronics as well as providing a simple method for controlling the graphene/dielectric interactions at the nanometre scale.

2. Experimental methods

2.1. Graphene growth and transfer

Graphene was grown by low pressure (LP) CVD using polycrystalline 25 μm thick (99.8% purity) copper foil using conditions similar to reports in the literature [9]. Graphene transfer was achieved by following the procedure proposed by Li *et al* [9] and Bhaviripudi *et al* [11]. The procedure consists of five different stages: (a) polymer spin-coating on one side of the graphene/Cu foil and subsequently using a cotton bud soaked with diluted nitric acid on the rear side of the Cu foil to remove the graphene; (b) etching of the Cu foil in an aqueous based solute ($FeCl_3$, 3.5 g in 10 ml of HCl and 100 ml of DI water); (c) 'washing' the graphene/polymer membrane by removal of the etchant solution and replacing it with DI water; (d) scooping the graphene/polymer membrane floating at the air/water interface using the desired substrate (i.e. glass or plastic); (e) removal of the polymer coating in an acetone bath at 55 °C for 15 min. An often overlooked graphene defect is the residual polymer. Here we optimized the cleaning of the graphene surface from the residual polymer using different polymers and adopting different polymer treatments and cleaning procedures as described in the supplementary information (SI; available at stacks.iop.org/Nano/23/344017/mmedia).

2.2. Transistor fabrication and characterization:

Graphene field-effect transistors based on SAM nanodielectrics were fabricated on glass and plastic substrates. In brief, 30 nm thick Al gate electrodes were deposited by vacuum sublimation through a shadow mask onto pre-cleaned glass substrates in high vacuum (10^{-6} mbar). The Al electrodes were then oxidized by oxygen plasma treatment (80 W for 30 s) in order to form a thin layer of native AlO_x approximately 5–10 nm thick. The Al–AlO_x gate electrodes were functionalized with the SAM nanodielectrics by dipping the substrates into the SAM solution. As expected, the surface morphology of the Al–AlO_x–SAM gate electrodes was found to be very similar to that of the bare Al–AlO_x. Details of the functionalization procedure have been reported elsewhere [13]. Gold source (S) and drain (D) electrodes were thermally evaporated through a shadow mask in high vacuum to define the transistor channel with dimensions in the ranges of 20–200 μm and 0.5–2 mm for the channel length and width, respectively. Devices based on Hyflon AD (Solvay) as the gate dielectric were realized by spin casting a thin layer of Hyflon AD directly onto Si^{++}/SiO_2 wafers followed by the transfer of the graphene layer and the thermal evaporation of the gold S–D electrodes. Electrical characterization of the transistors was performed at different atmospheric conditions using a Keithley 4200 semiconductor parameter analyser. Carrier mobilities were estimated using the standard field-effect transistor model in the linear operating regime (see SI available at stacks.iop.org/Nano/23/344017/mmedia).

3. Results and discussion

It is well established that charge transport in graphene devices is greatly affected by intrinsic graphene acoustic phonons, Coulomb impurities, surface roughness and surface polar phonon scattering from the contiguous dielectric [14, 15]. In addition, polar substrates such as SiO_2, a commonly used dielectric in graphene devices, that retain water molecules, adversely affect the charge transport across the device channel. The primary origin of the hydrophilicity of the SiO_2 surface is the dangling bonds that are often functionalized with hydroxyl groups (–OH), which are very hydrophilic and attract water molecules. These molecules can modify the charge transfer at the SiO_2/graphene interface, which often results in extrinsic p-type doping of the graphene layer. Furthermore, carrier mobility degradation, Dirac voltage shift and operating hysteresis are commonly observed leading to electrical instabilities of the graphene transistors under test. In order to reduce these undesired effects and further improve the charge carrier transport within the channel, the graphene/dielectric interface has to be carefully engineered and optimized.

Here we have investigated the effect of an amorphous fluoropolymer (Hyflon AD 3.6%) inserted between the graphene layer and the SiO_2 dielectric on the transistor characteristics. Hyflon AD is a proprietary amorphous perfluoropolymer from Solvay comprising of a copolymer of tetrafluoroethylene and a dioxole. Hyflon AD is transparent, highly hydrophobic (water contact angle $\sim$ 117°) (figure 1) and is characterized by a very low permittivity ($\varepsilon \sim 2$). For the purpose of this study the perfluoropolymer was deposited onto 400 nm of SiO_2 by spin-coating a solution of Hyflon AD (3.6%) diluted in Galden (1:5). Due to its very high hydrophobicity, the graphene/Hyflon AD interface is expected to lead to better transistor performance than conventional SiO_2/graphene based devices. In an effort to elucidate the kinetics of water adsorption onto these very different graphene/dielectric interfaces, electrical measurements were performed under three different atmospheres: air, N_2 and vacuum. The transistors were then annealed at 200 °C for 1 h in N_2 to remove any residual water molecules followed by electrical characterization. This measurement protocol enabled comparison of the effects of the ambient atmosphere and thermal annealing treatment on transistor operation.

Typical sets of transfer characteristics obtained from graphene transistors based on bare SiO_2 (control device) and SiO_2/Hyflon AD dielectric in N_2 and vacuum, before and after thermal annealing, are shown in figures 2(a) and (b).

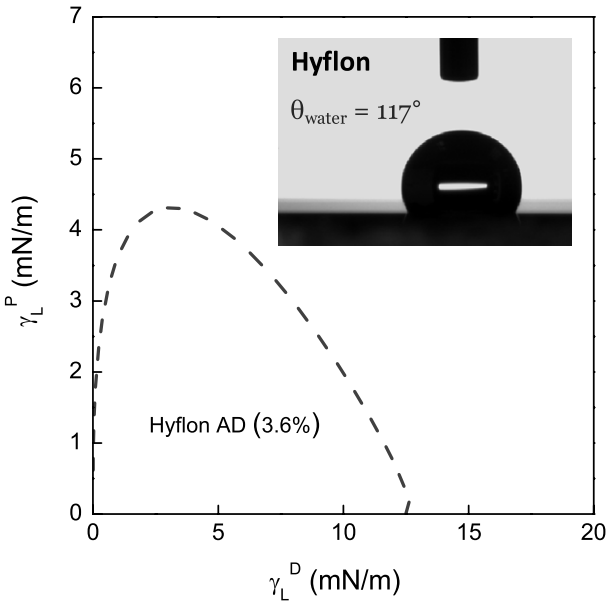

Figure 1. The wetting envelope ($\theta = 0°$) calculated for the SiO_2/Hyflon AD surface. Inset: image of the contact angle (119°) between a water droplet and Hyflon AD.

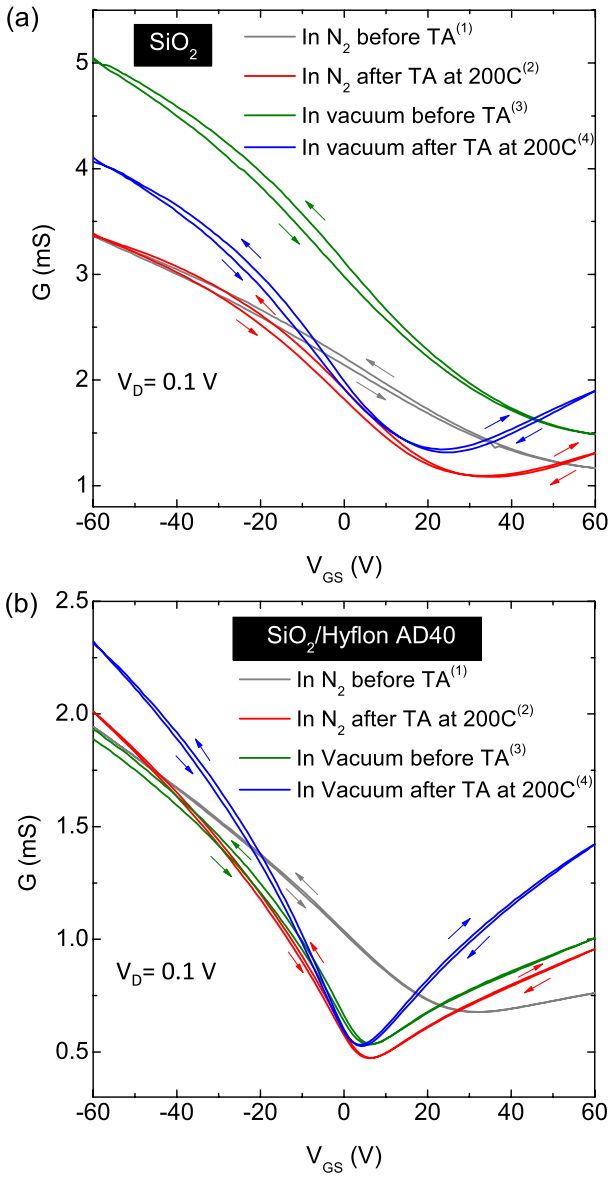

Figure 2. Transfer characteristics of transistors based on (a) bare SiO_2 (control device) and (b) SiO_2/Hyflon AD as the gate dielectric. Electrical characterization of the devices was performed in N_2 atmosphere (1—grey line), after annealing at $T = 200\,°C$ for 1 h (2—red line) and in vacuum after a short exposure to ambient air before (3—green line) and after annealing at $T = 200\,°C$ for 1 h (4—blue line). The maximum channel transconductance on/off ratio for the SiO_2 based transistor was 4.4 and was measured after vacuum annealing at 200 °C. SiO_2/Hyflon based transistors show a maximum channel transconductance on/off ratio of 3.3 after annealing at 200 °C in N_2.

It can be seen that as-prepared graphene transistors based on SiO_2 exhibit p-doping characteristics as evidenced by the very positive Dirac point potential (>60 V). Because of this severe extrinsic p-doping behaviour only hole accumulation can be observed. After thermal annealing at 200 °C for 1 h, the Dirac point is found to shift to ∼34 V, with the graphene channel remaining significantly p-doped. When measured in vacuum after a short exposure to air (∼5 min), the Dirac point shifts back to the values measured in as-prepared devices (>60 V). This set of measurements demonstrates the pivotal role that water molecules play on the doping characteristics of the SiO_2/graphene channel. When the same SiO_2/graphene based transistors are subjected to thermal annealing at 200 °C in vacuum for 1 h, the Dirac point shifts to ∼24 V and the corresponding charge density decreases to 1.29×10^{12} cm^{-2}. The latter value represents the lowest level of doping measured in our SiO_2/graphene transistors.

As-prepared graphene transistors based on the SiO_2/Hyflon AD dielectric, on the other hand, exhibit a lower Dirac point voltage (∼31 V) when compared to SiO_2/graphene based devices (i.e. >60 V). This indicates an improved (more inert) graphene/dielectric interface. After thermal annealing at 200 °C for 1 h (in N_2) the transistors exhibit an almost neutral behaviour with a Dirac point close to 6 V. When the transistor is exposed to air for 5 min, the Dirac point increases slightly to 8 V, while re-annealing the devices in vacuum at 200 °C yields a Dirac point close to ∼4 V. This value corresponds to a charge density of 1.32×10^{11} cm^{-2}, i.e. a value nearly one order of magnitude lower than that derived for SiO_2 based transistors. Therefore, it can be concluded that in the case of fluoropolymer/graphene interfaces, the extrinsic p-doping is significantly reduced and the charge neutrality of the graphene can be maintained. The latter observation is most likely attributed to the highly hydrophobic nature of the Hyflon AD polymer, which prevents the absorption of water at the dielectric/graphene interface.

A further important characteristic is the negligible operating hysteresis observed in SiO_2/Hyflon AD based transistors when compared to bare SiO_2 based devices. Interestingly, the hysteresis is clockwise under electron accumulation and anticlockwise under hole accumulation. This is most likely attributed to charge carrier injection from the graphene to the graphene/dielectric interface [15]

Table 1. Summary of the operating parameters measured for CVD graphene transistors based on SiO_2 and SiO_2/Hyflon AD as the gate dielectric in nitrogen and vacuum. The transistor parameters were obtained before and after thermal annealing at 200 °C for 1 h. The values in parentheses for the neutrality point correspond to the Dirac point in the reverse sweep.

			Charge carrier mobility ($cm^2\ V^{-1}\ s^{-1}$)			
	Atmosphere	Annealing (°C)	Electrons	Holes	Dirac point (V)	G_{max}/G_{min}
SiO_2/GR	N_2	As prepared	—	410	>60	2.6
	N_2	200	300	660	34 (34)	3.1
	Vacuum	As prepared	—	670	>60	3.4
	Vacuum	200	360	790	23 (25)	3.1
SiO_2/Hyflon/GR	N_2	As prepared	126	632	31 (33)	2.9
	N_2	200	423	1210	6 (7)	4.3
	Vacuum	As prepared	406	1151	6 (7)	4.1
	Vacuum	200	703	1435	4 (4)	4.4

although further work would be required in order to verify the exact mechanism. By comparing the operating characteristics of the two types of devices after annealing (200 °C) in vacuum, further differences can be identified. For example, SiO_2/Hyflon AD transistors show much more pronounced ambipolar transfer characteristics when compared to bare SiO_2 based transistors although the channel conductance of SiO_2/Hyflon AD devices is lower than that measured for SiO_2 based transistors. This is attributed to the lower geometrical capacitance of the SiO_2/Hyflon AD dielectric layer ($C_i \sim$ 5.3 nF cm^{-2}) when compared to bare 400 nm thick SiO_2 ($\sim$8.6 nF cm^{-2}). More importantly, graphene transistors based on SiO_2/Hyflon AD exhibit a maximum carrier mobility of $\sim$1400 $cm^2\ V^{-1}\ s^{-1}$ while for devices based on bare SiO_2 a maximum mobility value of 1000 $cm^2\ V^{-1}\ s^{-1}$ has been obtained. This significant difference can be ascribed mainly to charged impurities present at the graphene/SiO_2 interface. In addition to higher carrier mobilities, graphene transistors based on SiO_2/Hyflon AD also exhibit higher channel transconductance on/off ratios with maximum values around 4.4 (measured in vacuum after thermal annealing at 200 °C). Upon brief exposure to ambient air (2–3 min), transistors based on SiO_2/Hyflon AD exhibit negligible shift in the Dirac point, whereas in the case of bare SiO_2 based devices the Dirac point shifts significantly to positive gate voltages and the graphene channel exhibits strong p-doping characteristics. Based on these results it can be concluded that in the case of solution processed graphene transistors, passivation of the SiO_2 surface with a non-polar polymer such as Hyflon AD leads to a significant improvement in transistor operation and specifically higher charge carrier mobility and improved channel transconductance on/off ratio. Table 1 summarizes the various operating parameters of our graphene transistors based on bare SiO_2 and SiO_2/Hyflon AD measured at different experimental conditions.

In order to better understand the impact of atmospheric oxidants on the long term stability, both bare SiO_2 and SiO_2/Hyflon AD based transistors were exposed to air for prolonged periods of time. Electrical measurements were then obtained at regular intervals over a period of six weeks during which the relative humidity (24–60%) and ambient temperature (18–22 °C) were recorded. Figure 3 displays the transfer characteristics for the two types of devices (i.e. graphene transistors based on SiO_2, figure 3(a), and on SiO_2/Hyflon, figure 3(b)) obtained in vacuum and after exposure to ambient air for 5 min, 1 h, 1 day, 1 week, 3 weeks and 5 weeks. For the bare SiO_2 based graphene transistors, the Dirac point is found to shift by more than 60 V within the first 5 min of exposure (figure 3(a)). On the other hand, the Dirac point in graphene transistors based on SiO_2/Hyflon AD has increased by only 20 V after being exposed to air for 1 day; 30 V after exposure for 2 weeks; and 40 V after exposure for 6 weeks (figure 3(b)). The evolution of the Dirac point as a function of exposure time is shown in figure 3(c). The latter plot demonstrates the important advantage of SiO_2 surface passivation with Hyflon AD as it significantly improves the air stability of the transistors. It can also be concluded that water absorption is much slower in graphene transistors based on Hyflon AD than for devices based on bare SiO_2. We emphasize that the same device trends have been observed for a large number of transistors with relatively small deviations.

Although the passivation of SiO_2 with Hyflon AD provides a viable route towards high performance graphene transistors, it can clearly be seen from figures 2 and 3 that the resulting devices operate at relatively high voltages. In an effort to reduce the operating voltage of our graphene transistors we have explored the use of ultra-thin (2–3 nm) self-assembled monolayer (SAM) nanodielectrics functionalized directly onto suitable gate electrodes. It has been shown that the use of such organic SAMs [16, 17] enables the fabrication of low voltage (<|2| V) transistors based on a range of organic semiconductors as well as fullerene derivatives [16, 18]. However, despite the simplicity and potential of this approach, SAM dielectrics have never been used for realizing low voltage graphene transistors.

Using this early work as our starting point we have explored the potential of two different organic SAMs as nanodielectrics in our graphene transistors processed at temperatures below 140 °C. The SAM molecules used consist of a phosphonic acid as the anchoring group, a linear aliphatic chain with tunable molecular lengths as spacers, and a methyl or a carboxyl group as the end groups. Figure 4(a) shows the molecular structure of the two SAMs, namely octadecylphosphonic acid (ODPA) and

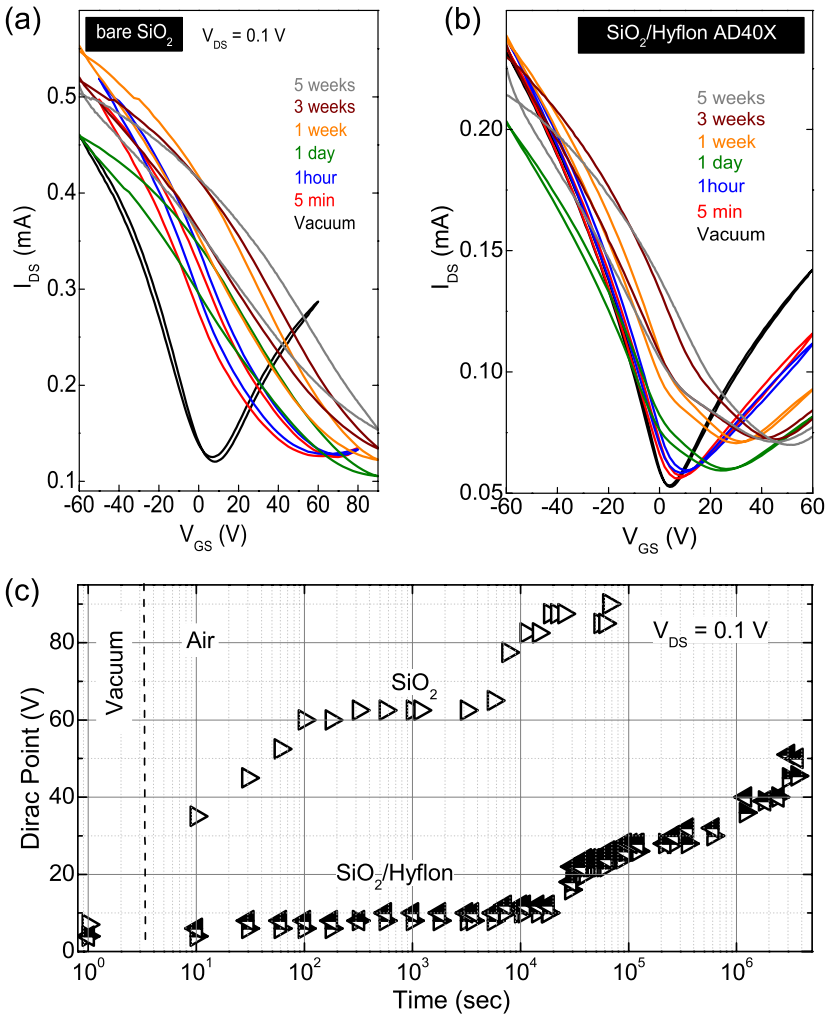

Figure 3. Transfer characteristics obtained from (a) transistors based on bare SiO_2 (control device), and (b) from transistors based on SiO_2/Hyflon AD. Measurements were performed for different exposure times to ambient air. (c) The evolution of the Dirac point potential (V_G) as a function of exposure time to ambient air.

phosphonohexadecanoic acid (PHDA), used in this study. The ODPA and PHDA molecules are characterized by the highly hydrophobic methyl (–CH_3) and highly hydrophilic carboxyl (–COOH) end groups, respectively. The SAMs were deposited by submerging the gate electrode containing substrates in a 5 mM solution of the corresponding SAM in isopropanol. Subsequently, the substrates were annealed for 12 h at 140 °C in nitrogen atmosphere. To verify the formation of a SAM, the surface energy of the functionalized gate electrode was measured using the Owens–Wendt–Kaelble method [19]. Figure 4(b) shows the $\theta = 0°$ wetting envelopes for the surfaces of the gate electrodes functionalized with the ODPA and PHDA SAMs together with the representative contact angle images [20, 21]. As expected, the ODPA functionalized electrode is found to be highly hydrophobic ($\theta \sim 109°$) with low surface energy mainly dominated by dispersive (non-polar) interactions. The surface of the PHDA functionalized electrode on the other hand is found to be hydrophilic ($\theta \sim 60°$) and exhibits relatively large surface energy characteristics (figure 4(b)) [13, 21]. These results suggest that the SAMs are uniformly deposited forming a dense monolayer. It is worth noting that once the phosphonic SAMs are functionalized onto the native AlO_x, they appear to be thermally stable for temperatures up to 300 °C (verified by contact measurements and current–voltage measurements). The high coverage of the Al–AlO_x gate electrode with the SAM was further verified by current (J)–voltage (V) measurements where the leakage current between two metal electrodes in a metal/SAM/metal structure was found to reduce from 10^{-3} A cm^{-2} (i.e. no SAM: Al–AlO_x/metal) to less than 10^{-8} A cm^{-2} at 1 V upon SAM functionalization (i.e. Al–AlO_x/SAM/metal) [20]. Using similar metal/SAM/metal structures, the geometrical capacitances (C_i) of devices based on ODPA and PHDA have also been measured yielding values in the ranges of 450 nF cm^{-2} and 550 nF cm^{-2}, respectively.

Figures 5(a) and (b) display the channel transconductance (G) as a function of gate voltage (V_G) for graphene transistors based on ODPA and PHDA nanodielectrics, respectively. Hysteresis free operation along with a high transconductance on/off ratio (G_{max}/G_{min}) of 5–6 and a lower level of p-doping than SiO_2/Hyflon AD transistors is observed for

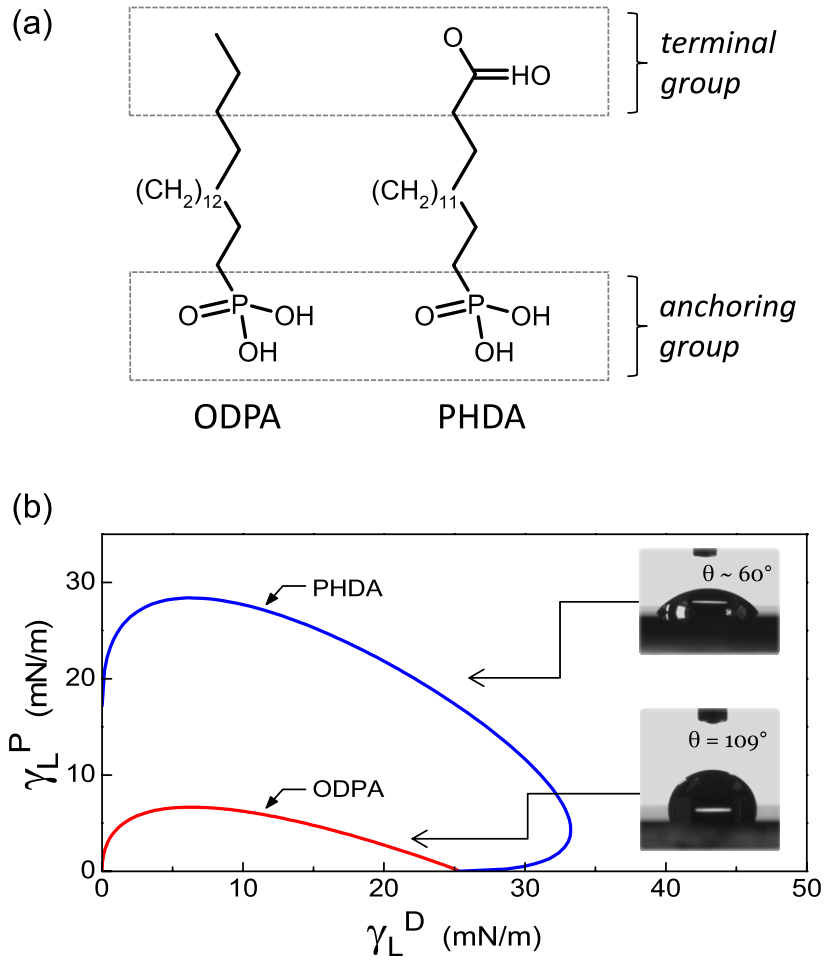

Figure 4. (a) Molecular structures of the ODPA and PHDA SAM dielectrics used. (b) Wetting envelopes calculated for ODPA and PHDA treated electrodes at $\theta = 0°$. Inset: images of water droplets on Al–AlO_x/ODPA and Al–AlO_x/PHDA surfaces showing contact angles of 109° and 60°, respectively.

both SAM based devices. Although transistors based on both SAMs exhibit ambipolar transport, holes are moderately more mobile than electrons especially in the PHDA/graphene interface. In particular, ODPA based transistors exhibit higher maximum hole ($\mu_h \sim 637$ cm^2 V^{-1} s^{-1}) and electron ($\mu_e \sim 372$ cm^2 V^{-1} s^{-1}) mobilities than PHDA based graphene transistors ($\mu_h \sim 351$ cm^2 V^{-1} s^{-1} and $\mu_e \sim 251$ cm^2 V^{-1} s^{-1}). The superior characteristics of the ODPA/graphene devices as compared to PHDA can be understood in the light of the prediction that low polarity substrates [22] are beneficial for optimizing the carrier mobility in graphene. In the present case, the mobilities are adversely affected by the high surface roughness of the substrate and by the different graphene topographic features (see the discussion below and the supplementary information available at stacks.iop.org/Nano/23/344017/mmedia) [23]. It is also worth mentioning that the dipole moment of the SAM's terminal group (i.e. methyl, carboxyl termination) affects the electrical characteristics of the graphene transistors through a noticeable shift in the neutrality point [24, 25]. Specifically, a downshift of the threshold voltage (V_{TH}) of −0.5 V is observed for positive V_D, and −1 V for negative V_D bias (figure 5(a)). The shift is highly reproducible and observed in all ODPA based graphene transistors. This may be attributed to the additional local field generated by the SAM surface [24, 25]. That is, the ordering of SAM molecules where molecular dipoles produce a built-in electric field superimposed over the externally applied gate field. This built-in field could shift the threshold voltage due to the modification in the carrier density within the transistor channel. This result suggests that CH_3–SAM molecules generate a local electric field that enhances electron accumulation. Similar observations have been reported by Yan *et al* [23].

Table 2 summarizes the carrier mobilities and threshold voltages reported in the literature for graphene transistors based on bare SiO_2 and SAM treated SiO_2 as the gate dielectric. For CVD graphene transistors based on SiO_2–SAM, the charge carrier mobility varies between 200 cm^2 V^{-1} s^{-1} [23] and 12 000 cm^2 V^{-1} s^{-1} [12]. This large variation suggests sensitivity towards both the processing of the SiO_2 and its surface treatment with the SAM. From this table it can also be concluded that our results are in line with previously published data as regards the importance of the dielectric surface. However, in the present study the SAMs do not only alter the electrostatic landscape of the dielectric–graphene interface but in addition define the overall dielectric thickness. This is a key feature of our approach as it allows fabrication of

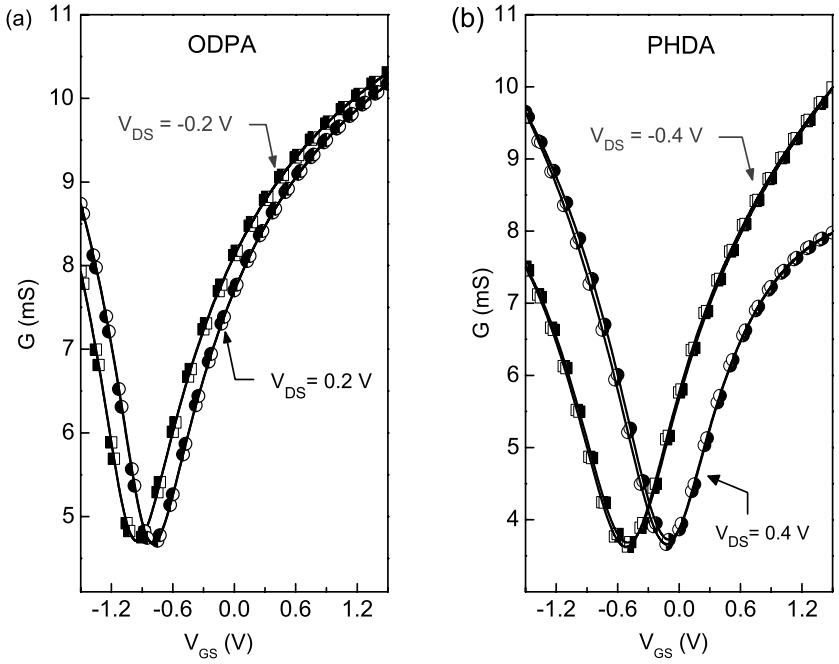

Figure 5. Transfer characteristics measured for solution processed graphene transistors based on different SAM nanodielectrics. (a) Transfer characteristics obtained from ODPA based devices and (b) those from PHDA based devices. The channel length (L) and width (W) are $W/L = 1000/30$ μm and $W/L = 1500/40$ μm for the ODPA and PHDA based transistors, respectively. ODPA based transistors exhibit a maximum channel transconductance on/off ratio of 3.4 while PHDA based transistors exhibit ∼2.8.

Table 2. Summary of performance parameters reported in the literature for graphene transistors based on bare SiO_2 and on SiO_2 treated with different SAMs.

	Transistor parameter	
Source	Charge carrier mobility (cm^2 V^{-1} s^{-1})	Threshold voltage V_{TH} (V)
Reference [13]: SiO_2–PBTS	2 500	40
Reference [13]: bare SiO_2	1 000	40
Reference [12]: SiO_2–HMDS	12 000	∼50
Reference [12]: bare SiO_2	4 000	∼50
Reference [23]: SiO_2–H_2N	661	−18
Reference [23]: SiO_2–CH_3	460	−8
Reference [23]: SiO_2–H_3N^+	363	20
Reference [23]: bare SiO_2	449	4
Reference [23]: SiO_2 treated with CF_3	450	30

graphene transistors capable of operating at very low voltages (<|1.5| V). To our knowledge this is the first demonstration of low operating voltage graphene transistors based on these solution-processable SAM nanodielectrics.

In the case of PHDA based graphene transistors, a negative shift in the V_{TH} between −0.5 V and −0.3 V (figure 5(b)) for negative and positive V_D, respectively, was observed. Taking into account the built-in electric field model interaction, a positive shift of the neutrality point may be expected, as the hydroxyl groups are known to act as electron traps [14, 26]. However, charge transfer from the PHDA to the graphene could be a competitive mechanism, leading to a negative shift of the threshold voltage as observed in similar systems formed by carbon nanotubes (as well as fullerene derivatives) in close proximity with carboxylic groups [20]. It can thus be concluded that suitably engineered SAMs can be used to dope the graphene channel via electric dipoles and charge transfer mechanisms without compromising the charge carrier mobility through the introduction of charge scattering centres. Despite the early stage of this research it can be argued that the presence of long aliphatic chains at the graphene interface appears to be more beneficial to the electrical characteristics of graphene transistors than the presence of a polyfluorinated polymer as the passivation layer.

In order to demonstrate the compatibility of the low voltage CVD graphene devices with flexible plastic substrates we have fabricated ODPA and PHDA based transistors on polyethylene terephthalate (PET) substrates. Figures 6(a) and (b) display the transfer characteristics for devices based on PHDA and ODPA SAM nanodielectrics, respectively, while figure 6(c) shows a photograph of a set of graphene devices (>60) fabricated onto PET substrates. It can be seen that the substrate/transistor structure is highly flexible while the devices exhibit clear transistor behaviour and low voltage operation. The hole and electron mobilities extracted from the flexible devices are lower than those measured from graphene transistors fabricated on rigid glass substrates (i.e. figure 5). In particular, PHDA based devices show balanced hole/electron mobilities with maximum values of the order of 100 cm^2 V^{-1} s^{-1} while transistors based on ODPA exhibit lower performance with hole and electron mobilities of the order of 30 cm^2 V^{-1} s^{-1}. The low charge mobility values are most likely attributable to the incompatibility of the PET substrates with some of the processing steps employed during the graphene transfer and the subsequent device washing

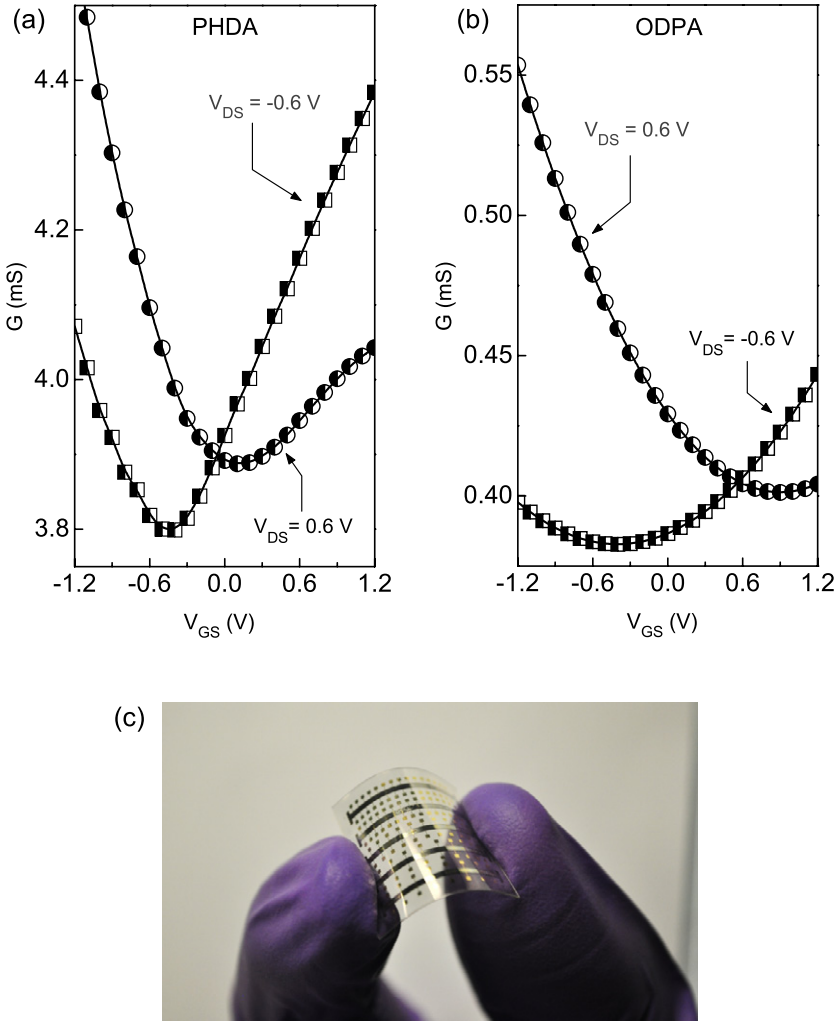

Figure 6. Transfer characteristics measured from graphene transistors based on SAM nanodielectrics fabricated on flexible plastic (polyethylene terephthalate (PET)) substrates. Transfer characteristics measured for PHDA (a) and ODPA based (b) graphene transistors. (c) Photograph of a set (35 devices) of ODPA SAM based CVD graphene transistors fabricated on PET substrates.

steps. Washing the devices with acetone, in particular, was found to affect the PET surface and the overall integrity of the Al–AlO_x/SAM electrode. An alternative process or use of a different type of plastic could in principle be employed to circumvent this problem. However, this is beyond the scope of this work and should be the subject of future studies.

An interesting observation that is worth mentioning is that the operating characteristics of SiO_2 based graphene transistors closely resemble those obtained by Aguirre *et al* for carbon nanotube (CNT) transistors based on SiO_2 [25]. In the latter study the workers observed a reduction in the electron conduction in the CNTs upon adsorption of a water layer containing solvated oxygen present on the SiO_2 surface. A similar effect is clearly observed in our SiO_2 based graphene transistors where the n-type conduction is found to reduce upon exposure to air (see table 1). This confirms that the electrochemically mediated charge transfer to the O_2/H_2O redox couple appears to be ubiquitous in many different semiconductor materials.

In order to understand the origin of the difference in performance observed between Al–AlO_x/SAM and SiO_2/Hyflon based transistors one must also consider the dielectric–graphene surface topography. Figure 7 displays tapping mode AFM images of the surface topography for SiO_2/Hyflon/graphene (a)–(b), Al–AlO_x/ODPA/graphene (c)–(d) and, for comparison, SiO_2/graphene (e)–(f). In all the samples, the transferred graphene layer covers the entire substrate (see SI, figure S3 available at stacks.iop.org/Nano/23/344017/mmedia). Importantly, the large range scans shown in figures 7(a), (c) and (e) reveal substantially different graphene topographies. This is most likely attributable to graphene delamination which progressively decreases with increasing dielectric surface energy, i.e. from highly hydrophobic Hyflon AD (figure 7(a)) to highly hydrophilic SiO_2 (figure 7(e)), as well as with increasing dielectric roughness (figure S2 available at stacks.iop.org/Nano/23/344017/mmedia). In particular, wide bulged areas are visible on the SiO_2/Hyflon/graphene (figure 7(a)), while narrow elongated wrinkles are present in the case of the SiO_2/graphene (figure 7(e)), with the exception of some isolated bulges. This conformal nature of the graphene layer on SiO_2 is in agreement with prior observations [28] and

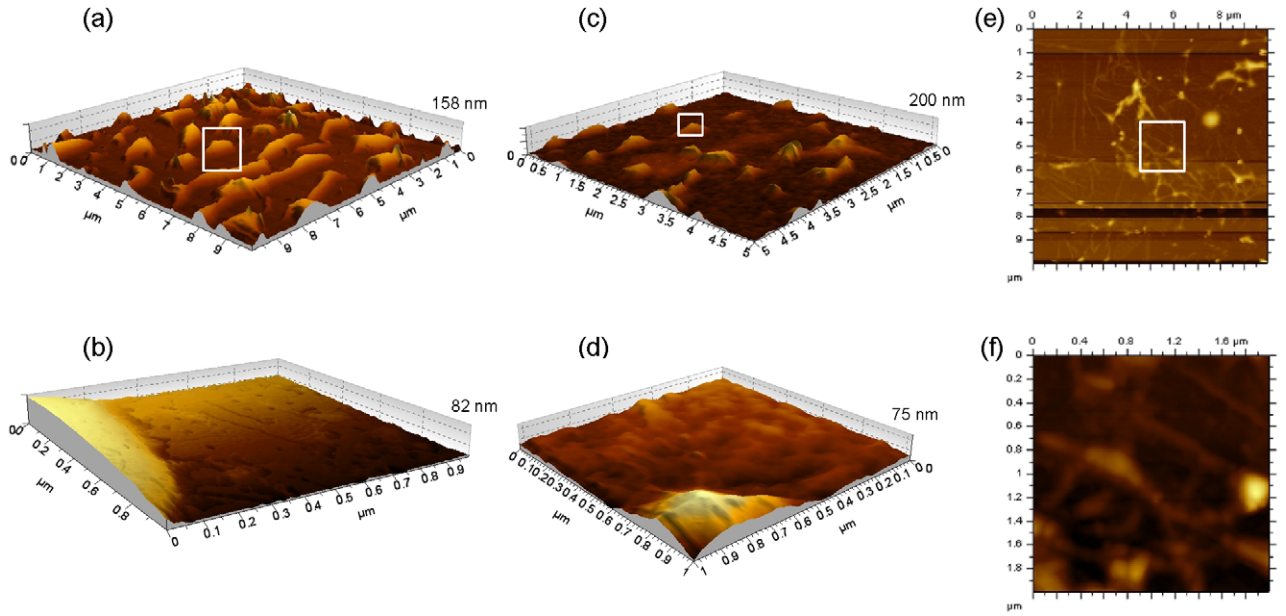

Figure 7. Tapping mode AFM images of the topography of the different surfaces. (a) Large area scan of SiO_2/Hyflon/graphene. (b) Small area scan of SiO_2/Hyflon/graphene identified by the white rectangle in (a). (c) Large area scan of Al–AlO_x/ODPA/graphene. (d) Small area scan of Al–AlO_x/ODPA/graphene identified by the white rectangle in (c). (e) Large area scan of SiO_2/graphene. (f) Small area scan of SiO_2/graphene identified by the white rectangle in (e).

is most likely attributable to the smoothness (figure S2(a) available at stacks.iop.org/Nano/23/344017/mmedia) [27] and high surface energy of SiO_2. The extensive delamination observed in solution-transferred graphene on hydrophobic surfaces such as Hyflon AD further supports the idea that interfacial adhesion interactions, as well as surface roughness, play a pivotal role. Based on these observations it can also be argued that extended delamination detaches the graphene from the dielectric surface therefore limiting the extrinsic scattering of charge carriers and increasing their mobility. This is in agreement with the experimental data summarized in table 1 where Hyflon AD based devices show consistently higher charge carrier mobilities as compared to bare SiO_2 based transistors. Further studies are underway to determine the role of the interfacial adhesion energy of graphene on different substrates [29, 30] and its dependence on the surface roughness.

4. Summary

In summary, we have demonstrated that graphene transistors based on SiO_2 passivated by a thin fluoropolymer film exhibit better electrical characteristics than bare SiO_2 based devices. The improvements include lower extrinsic p-doping, air stability over weeks, improved charge carrier mobility, higher channel transconductance on/off ratio and reduced operating hysteresis. These improvements have been attributed to the highly hydrophobic properties of Hyflon AD which prevent absorption of water molecules at the graphene/dielectric interface as well as in its peculiar surface morphology. Furthermore, we have shown that similar results can be obtained by replacing the SiO_2/Hyflon AD layer with carefully engineered ultra-thin SAM nanodielectrics. Because of the molecular scale of the dielectric thickness (<3 nm), graphene transistors based on these SAMs operate at low voltages and typically $<|1.5|$ V. By combining the SAM nanodielectrics with plastic substrates we have also been able to demonstrate flexible low voltage graphene transistors with promising operating characteristics. The unique combination of high mobility and low operating voltage coupled with the solution processability of SAMs at low temperatures makes our approach attractive for the development of low-power graphene electronics over large areas using low-cost substrate materials and processing methodologies.

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